IN THE CLAIMS:

Claims 1-8 (Cancelled).

9. (New) A semiconductor device comprising:

an instruction memory storing for associating, with an address, an instruction program comprising a plurality of instruction codes, and storing therein such instruction program as data;

an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes thereof;

a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal; and

an execution block for executing an instruction according to a control signal outputted from the decode block, and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction, wherein

when the instruction fetch block performs the fetch process, one of a branch address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory.

10. (New) The semiconductor device according to claim 9, wherein a branch address has a value obtained by adding a value of an address for reading out an instruction program and a value of displacement information included in such instruction program.

11. (New) The semiconductor device according to claim 9, further comprising a conditional branch instruction determiner for determining whether or not a conditional branch instruction is present in an instruction code outputted from the instruction fetch block, wherein

when the conditional branch instruction determiner detects a conditional branch instruction and outputs a signal indicating execution of such conditional branch instruction, address selection based on a conditional-branch-taken signal is performed, and

when the conditional branch instruction determiner detects no conditional branch instruction, address selection based on such conditional-branch-taken signal is not performed.

12. (New) The semiconductor device according to claim 9, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array including a plurality of memory cells specified based on an output from the X decoder and an output from the Y decoder,

the X decoder having an input address specified by an upper bit of an address outputted from the instruction fetch block,

the Y decoder including a normal decoder for decoding a lower bit of an address outputted from the instruction fetch block,

a branch Y decoder for decoding a lower bit of a branch address having a same bit width as that of a lower bit of an address outputted from the instruction fetch block, and

a selector for receiving an output from the normal Y decoder and an output from the branch Y decoder, selecting one of the outputs according to a conditional-branch-taken signal outputted from the execution block and outputting a selected output, wherein

the lower bit of an address specifying one of the memory cells of the memory array is specified by an output from the selector.

13. (New) The semiconductor device according to claim 9, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array including a plurality of memory cells specified based on an output from the X decoder and an output from the Y decoder, the X decoder and the Y decoder having intput addresses set by addresses outputted from the instruction fetch block, and

the device further comprising a selector for selecting as an input address to the Y decoder, one of the branch addresses generated based on displacement information included in instruction program data and an address outputted from the instruction fetch block, based on a conditional-branch-taken signal outputted from the execution block, and outputting the selected address, wherein

a lower bit of an address specifying one of the memory cells of the memory array is specified by an output from the Y decoder.

14. (New) The semiconductor device according to claim 11, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array including a plurality of memory cells specified based on an output from the X decoder and an output from the Y decoder,

the X decoder having an input address specified by an upper bit of an address outputted from the instruction fetch block,

the Y decoder including a normal Y decoder for decoding a lower bit of the address outputted from the instruction fetch block,

a branch Y decoder for decoding a lower bit of a branch address having a same bit width as that of a lower bit of an address outputted from the instruction fetch block, and

a selector for receiving an output from the normal Y decoder and an output from the branch Y decoder, selecting one of the outputs according to a conditional-branch-taken signal outputted from the execution block and outputting the selected output, wherein

a lower bit of an address specifying one of the memory cells of the memory array is specified by an output from the selector.

15. (New) The semiconductor device according to claim 11, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array including a plurality of memory cells specified based on an output from the X decoder and an output from the Y decoder, the X decoder and the Y decoder having a plurality of input addresses set by addresses outputted from the instruction fetch block, and

the device further comprises a selector for selecting, as an input addresses to the Y decoder, one of the branch addresses generated based on displacement information included in instruction program data and an address outputted from the instruction fetch block, based on a conditional-branch-taken signal outputted from the execution block, and outputting the selected address, wherein

a lower bit of an address specifying one of the memory cells of the memory array is specified by the output from the Y decoder.

16. (New) The semiconductor device according to claim 9, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array including a plurality of memory cells specified based on an output from the X decoder and an output from the Y decoder, the X decoder and the Y decoder having input addresses set by addresses outputted from the instruction fetch block,

the Y decoder selects one of the branch addresses generated based on displacement information included in instruction program data and an address outputted from the instruction fetch block based on a conditional-branch-taken signal outputted from the execution block, and outputs the selected address, thereby designating a lower bit of an address for specifying one of the memory cells of the memory array, and

the memory array is configured to map an address of a conditional-branch-taken instruction in each of the instruction codes from the instruction fetch block and an address of a branch target instruction, so that address inputs to the X decoder become identical and address inputs to the Y decoder alone differ from each other.

17. (New) A linking method for performing address mapping for a memory array in a semiconductor device comprising an instruction memory comprising a memory array including a plurality of memory cells each specified by an upper bit and a lower bit of an address, the instruction memory associating, with an address, an instruction program comprising a plurality of instruction codes and storing therein such instruction program as data, the upper bit and the lower bit of the address being designated in the memory array to perform such instruction program read out from the memory array of the instruction memory,

said method comprising:

comparing addresses between a conditional branch instruction and a branch target instruction each of which is an instruction program stored in the memory array of the instruction memory,

determining whether or not a predetermined upper bit of a conditional branch instruction and an upper bit of the branch target address differ from each other, based on a result of an address comparison between a conditional branch instruction and a branch target instruction, and

re-mapping the address of a branch target so that no carry into the predetermined upper bit thereof is caused, thereby optimizing arrangements of the address of a conditional branch instruction and the address of a branch target instruction, when the predetermined upper bits of the address of a conditional branch instruction and an address of the branch target instruction are determined to differ from each other.